AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A semiconductor substrate device, comprising:

a first semiconductor substrate including a concave-convex surface, the concave-convex surface comprising a convex portion including a top surface;

a second semiconductor substrate having a non-glass thin film insulator on a surface thereof,

wherein the first semiconductor substrate and the second semiconductor substrate are brought together so that the top surface of the convex portion of the concave-convex surface of the first semiconductor substrate and the thin film insulator provided on the surface of the second semiconductor substrate contact each other with no circuit or device element located therebetween, to form ~~a cavity~~ a two-dimensional array of cavities in the semiconductor substrate device.

2. (Original) A semiconductor substrate device according to claim 1, wherein the concave-convex surface of the first semiconductor substrate is defined by a plurality of convex portions formed at equal intervals.

3-5. (Canceled)

6. (Currently amended) A semiconductor substrate device, comprising:

a first semiconductor substrate including a concave-convex surface, the concave-convex surface comprising a convex portion including a top surface; and

a second semiconductor substrate having a thin film oxide insulator on a surface thereof, the surface of the second semiconductor substrate on which the thin film oxide insulator is provided being implanted with hydrogen ions,

wherein the first semiconductor substrate and the second semiconductor substrate are brought together so that the top surface of the convex portion of the concave-convex surface of the first semiconductor substrate and the thin film oxide insulator provided on the ion implanted surface of the second semiconductor substrate contact each other with no circuit or device element located therebetween, to form a ~~cavity~~ two-dimensional array of cavities in the semiconductor substrate device.

7. (Currently amended) A semiconductor substrate device, comprising:

a first semiconductor substrate including a concave-convex surface, the concave-convex surface comprising a convex portion including a top surface;

a second semiconductor substrate having a thin film Si layer on a surface thereof,

wherein the first semiconductor substrate and the second semiconductor substrate are brought together so that the top surface of the convex portion of the concave-convex surface of the first semiconductor substrate and the thin film Si layer provided on the

second semiconductor substrate contact each other with no circuit or device element located therebetween, to form a ~~cavity~~ two-dimensional array of cavities in the semiconductor substrate device.

8. (Previously presented) A semiconductor device according to claim 1, wherein the thin film insulator comprises a silicon oxide film.

9. (Previously presented) A semiconductor device according to claim 1, wherein the thin film insulator comprises a thin-film silicon layer.

10. (Previously presented) A semiconductor device according to claim 1, wherein the concave-convex surface of the first semiconductor substrate is defined by a plurality of concave portions, wherein a width(s) of the concave portions narrows as the depth of the concave portions increases.

11. (Previously presented) A semiconductor device according to claim 10, wherein said plurality of concave portions are formed at equal intervals.

12. (Previously presented) The device of claim 1, wherein the non-glass thin film insulator has a thickness less than a thickness of the second semiconductor substrate on

which the thin film insulator is provided, and wherein the thin film insulator is not a semiconductor.

13. (Previously presented) The device of claim 7, wherein the thin film Si layer has a thickness less than a thickness of the second semiconductor substrate on which the thin film Si layer is provided.

14. (New) The device of claim 1, wherein the two-dimensional array of cavities serve as respective low dielectric constant portions so that parasitic capacitance generated between the first substrate and circuit elements on the second substrate is reduced.

15. (New) The device of claim 6, wherein the two-dimensional array of cavities serve as respective low dielectric constant portions so that parasitic capacitance generated between the first substrate and circuit elements on the second substrate is reduced.

16. (New) The device of claim 7, wherein the two-dimensional array of cavities serve as respective low dielectric constant portions so that parasitic capacitance generated between the first substrate and circuit elements on the second substrate is reduced.